800G_OSFP_SR8_Optical Module

Product Specification Data

Product Name: QM_800G_OSFP_SR8_Optical Module

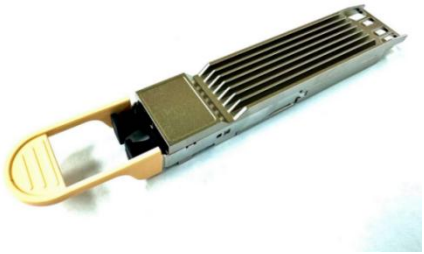
Part Number: 10001866

Record Number: TS09070

Version: A0

Date: 2025.02.24

Features



- Hot pluggable OSFP form factor
- Maximum link length of 100m on OM4 fiber with FEC
- +3.3V single power supply
- Power dissipation < 16W
- Operating case temp Commercial:0°C to+70 °C
- Dual MPO-12 APC connector
- RoHS compliant

Applications

- Application case 1,8x100G SR,8 of 100G per channel breakout connections
- Application case 2,2x400G SR4,2 of 400G per port breakout connections
- Application case 3,2x200G SR4,2 of 200G per port breakout connections
- Applications for backward compliance,refer to detailed application list below Mixed applications of case 1 and case 2 are also supported

Order Information

Table 1-Order Information

Part No.	Bit Rate (Gbps)	Laser (nm)	Distance note1	Fiber Type	DDMI	Connector	Temp note2
10001866	850	850	100m	MMF	YES	Dual MPO 1x12 APC	0℃~+70℃

Note:
1. OM4 fiber,60m for OM3 fiber,with FEC
2. Case Temperature

Absolute Maximum Ratings

Table2-Absolute Maximum Ratings

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Supply Voltage	V_{CC}	-0.5		+3.6	V	
Storage Temperature	T_s	-40		+85	℃	
Operating Humidity	*RH*	0		+85	%	1
Control Input Voltage	V_{in}	-0.3		V_{CC}+0.5	V	1

Note: 1 No condensation

Recommended Operating Conditions

Table 3- Recommended operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	T_c	0		+70	℃	
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Power Dissipation	P_d			14	W	
Supply Current	I_{CC}			4240	mA	
Pre-FEC Bit Error Ratio	-			$2.4x10^{-4}$	-	
Post-FEC Bit Error Ratio	-			$1x10^{-15}$	-	1
Link Distance (OM4)	-	2		100	m	2
Link Distance (OM3)	-	2		50	m	

Note:
1. FEC provided by host system
2. FEC required on host system to support maximum distance

Electrical Characteristics

Table 4-Electrical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Transmitter						
Signaling Rate per Lane	*SR*	53.125±100ppm			Gbd	

Modulation format	-	PAM4			-	
Differential pk-pk input Voltage tolerance	$V_{in,pp,diff}$	750			mV	
Effective return loss	*ERL*	8.5			dB	
Differential termination mismatch	-	-		10	%	
Single-ended voltage tolerance range	-	-0.4		3.3	V	
DC common-mode voltage tolerance	-	350		2850	mV	
Receiver						
Signaling Rate per Lane	*SR*	53.125±100ppm			Gbd	
Modulation format	-	PAM4			-	
Differential output Voltage(Long mode)	-			845	mV	
Differential output Voltage(Short mode)	-			600	mV	
Eye height	-	15			mV	
Vertical eye closure	*VEC*			12	mV	
Differential Termination Mismatch	-			10	%	
Transition Time	-	8.5			ps	
DC common mode Voltage tolerance	-	-350		2850	mV	

Table 5-Optical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Transmitter						
Signaling Rate per Lane	*SR*	53.125±100ppm			Gbd	
Modulation format	-	PAM4			-	
Center wavelength	λ_c	844	850	863	nm	
RMS Spectral Width	*SW*			0.6	dBm	
Average Launch Power per Lane	*AOP*	-4.6		4	dBm	1
Outer Optical Modulation Amplitude(OMA outer),each lane(min) For max(TECQ,TDECQ)≤1.8dB For 1.8<max(TECQ,TDECQ)≤4.4dB	*Tx OMA*	-2.6-4.4+max (TECQ,TDECQ)		3.5	dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ),each lane	*TDECQ*			4.4	dB	
Transmitter eye closure for PAM4,each lane	*TECQ*			4.4	dB	
Overshoot/undershoot	-			29	%	
Transmitter Transition Time	T_t			17	ps	
Average Launch Power of OFF Transmitter, each lane	T_{OFF}			-30	dBm	
$RIN_{14}OMA$	*RIN*			-132	dB/ Hz	
Extinction Ratio,each lane	*ER*	2.5			dB	
Optical Return Loss Tolerance	*ORL*			14	dB	
Encircled flux	-	≥86% at 19μm			dBm	2
		≤30% at 4.5μm				
Receiver						
Signaling Rate per Lane	*SR*	53.125±100ppm			Gbd	
Modulation format	-	PAM4			-	

Wavelength	*λ*	842	850	948	nm	
Damage Threshold,average optical power, each lane	*DT*	5			dBm	3
Average Receive Power,each lane	*RXPx*	-6.4		4	dBm	4
Receive Power (OMA) per Lane	*Rx OMA*			3.5	dBm	
Receiver Reflectance	*Rfl*			-15	dB	
Receiver Sensitivity (OMA outer),each lane	*SEN*			Max(-4.6,-6.2+TECQ)	dBm	5
LOS De-assert	*LOSD*			-6.6	dBm	
LOS Assert	*LOSA*	-15		-8.6	dBm	
LOS Hysteresis	*LOSH*	0.5			dB	

Note:
1. Average launch power,each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance
2. If measured into type A1a.2 or type A1a.3, or A1a.4, 50 µm fiber, in accordance with IEC 61280-1-4
3. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power
4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance
5. Measured with conformance test signal at TP3 for the BER equal to $2.4x10^{-4}$

Digital Diagnostic Specifications

Table 6-Digital Diagnostic Characteristics

Parameter	Symbol	Min.	Max.	Unit	Notes
Temperature monitor absolute error	DMI_Temp	-3	3	degC	Over operating temperature range
Supply voltage monitor absolute error	DMI_V_{CC}	-0.1	0.1	V	Over full operating range
Channel RX power monitor absolute error	DMI_RX_Ch	-3	3	dB	1
Channel Bias current monitor	DMI_Ibias_Ch	-10%	10%	mA	
Channel TX power monitor absolute error	DMI_TX_Ch	-3	3	dB	1

Notes:
1. Due to measurement accuracy of different multi-mode fibers, there could be an additional +/-1 dB fluctuation, or a +/-3 dB total accuracy

Recommended Interface

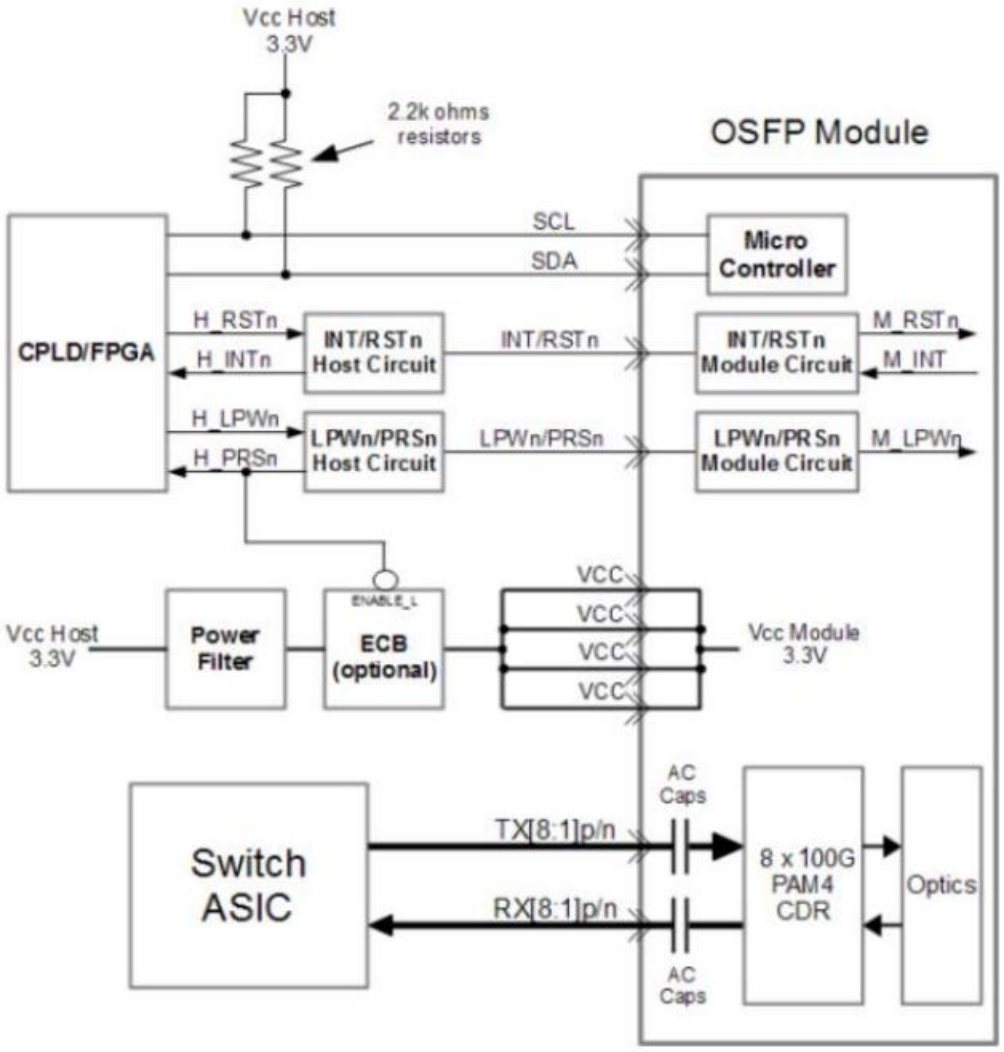


Figure 1, Recommended Interface Circuit

Pin arrangement

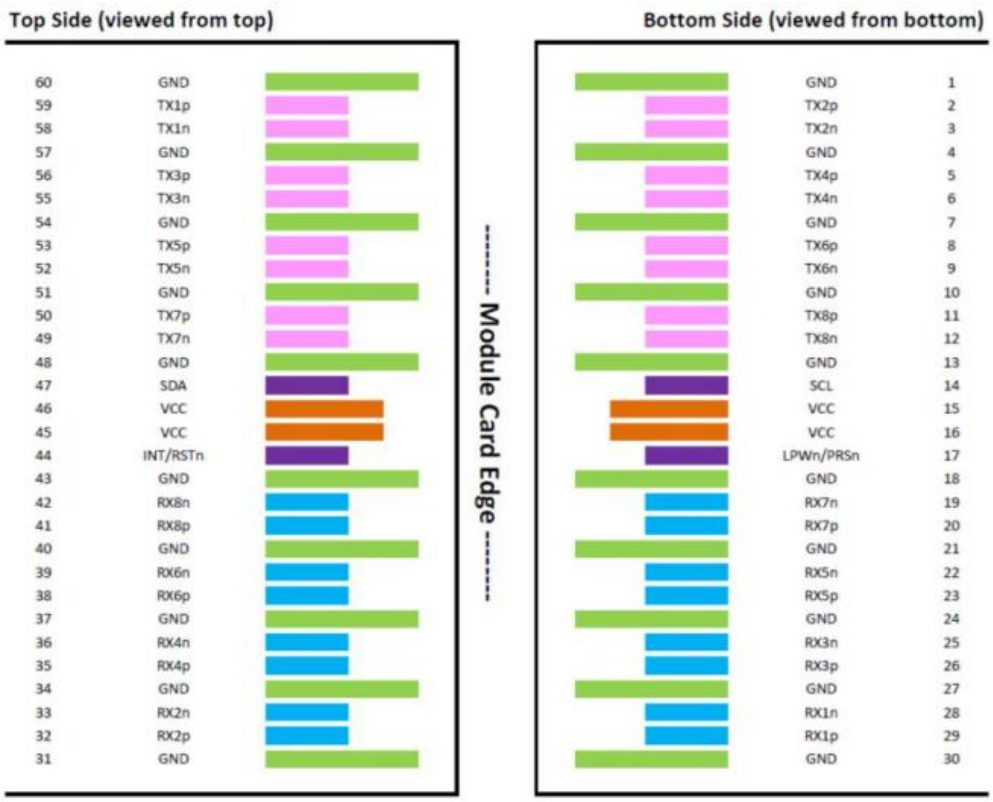


Figure 2, Pin View

Pin Function Definitions

Table 7-Pin Function Definitions

Pin	Symbol	Description	Logic	Direction	Plug Sequence
1	GND		Ground		1
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3
4	GND		Ground		1
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3
7	GND		Ground		1
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3
10	GND		Ground		1
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3
13	GND		Ground		1
14	SCL	2-wire Serial interface clock	LVCMOS-I/ O	Bi-directional	3
15	V_{CC}	+3.3V Power		Power from Host	2
16	V_{CC}	+3.3V Power		Power from Host	2

17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3
18	GND		Ground		1
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3
21	GND		Ground		1
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3
24	GND		Ground		1
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3
27	GND		Ground		1
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3
30	GND		Ground		1
31	GND		Ground		1
32	RX2p	Receiver Data Inverted	CML-O	Output to Host	3
33	RX2n	Receiver Data Non-Inverted	CML-O	Output to Host	3
34	GND		Ground		1
35	RX4p	Receiver Data Inverted	CML-O	Output to Host	3
36	RX4n	Receiver Data Non-Inverted	CML-O	Output to Host	3
37	GND		Ground		1
38	RX6p	Receiver Data Inverted	CML-O	Output to Host	3
39	RX6n	Receiver Data Non-Inverted	CML-O	Output to Host	3
40	GND		Ground		1
41	RX8p	Receiver Data Inverted	CML-O	Output to Host	3
42	RX8n	Receiver Data Non-Inverted	CML-O	Output to Host	3
43	GND		Ground		1
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3
45	V_{CC}	+3.3V Power		Power from Host	2
46	V_{CC}	+3.3V Power		Power from Host	2
47	SDA	2-wire Serial interface data	LVCMOS-I/ O	Bi-directional	3
48	GND		Ground		1
49	TX7n	Transmitter Data Non-Inverted	CML-I	Input from Host	3
50	TX7p	Transmitter Data Inverted	CML-I	Input from Host	3
51	GND		Ground		1
52	TX5n	Transmitter Data Non-Inverted	CML-I	Input from Host	3
53	TX5p	Transmitter Data Inverted	CML-I	Input from Host	3
54	GND		Ground		1
55	TX3n	Transmitter Data Non-Inverted	CML-I	Input from Host	3
56	TX3p	Transmitter Data Inverted	CML-I	Input from Host	3
57	GND		Ground		1
58	TX1n	Transmitter Data Non-Inverted	CML-I	Input from Host	3
59	TX1p	Transmitter Data Inverted	CML-I	Input from Host	3
60	GND		Ground		1

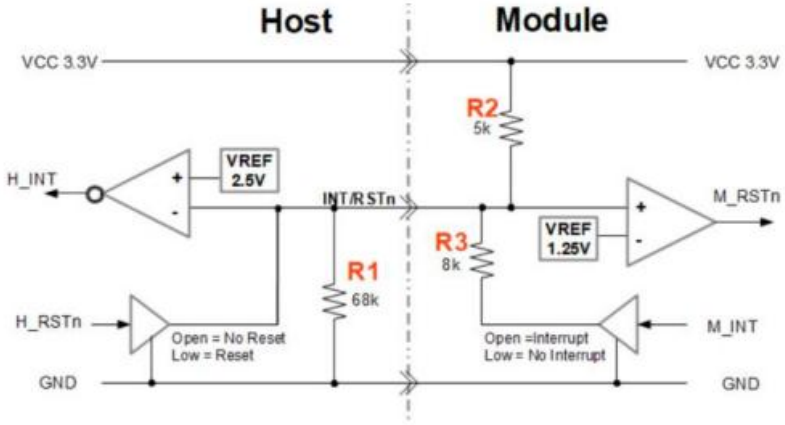


Figure 3,INT/RSTn circuit

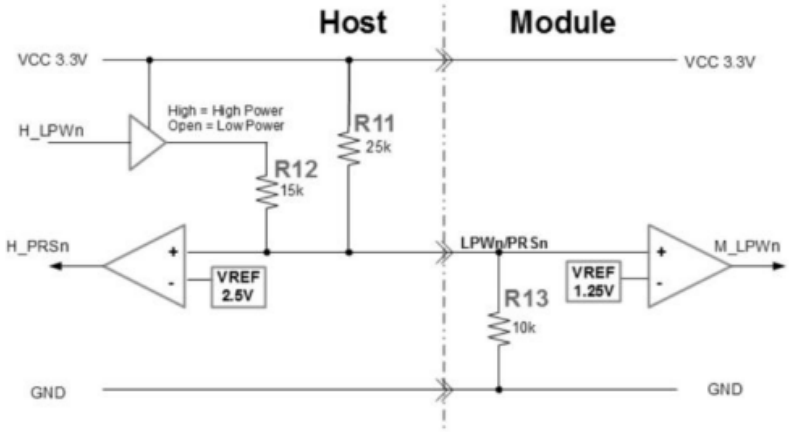


Figure 4,LPWn/PRSn circuit

Memory Map

Compatible with CMIS rev 5.2.

Optical interface arrangement

The optical port is dual MPO-12 APC connector receptacle, with fiber lane assignments as shown in Figure 5

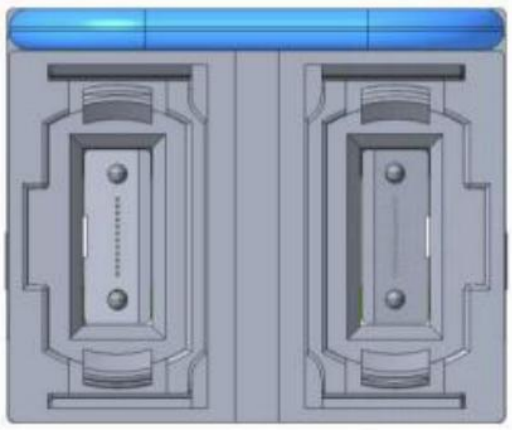


Figure 5,Optical interface arrangement.

Mechanical

800G SR8 OSFP transceivers are compatible with OSFP Module Specification Rev5.0 for pluggable form factor module.

Product list

Part Number	Product Name
10001866	光模块_850nm_800G_OSFP_SR8_50m_2*MPO-12_1*8_J97