QM 400G QSFP-DD AOC Optical Module

Product Specification Data

Product Name: QM_400G_QSFP-DD_AOC_Optical Module

Part Number: 1000XXXX

Record Number: TS09061

Version: A1

Date: 2025.02.24

Features

- Hot pluggable QSFP-DD form factor
- Case temperature range of 0℃to +70℃
- +3.3V single power supply
- Power dissipation < 10W per terminal
- Operating case temp
  Commercial: 0°C to +70 °C
- 8x50G PAM4 retimed 400GUAI-8
  electrical interface aligned with IEEE 802.3bs
- RoHS compliant

Applications

- 200GAUI-4
- Other 400G optical links

Order Information

Table 1-Order Information

Part No.	Bit Rate (Gbps)	Laser (nm)	Distance	Fiber Type	DDMI	Connector	Temp[note1]	Modulation
1000XXXX	8x53.125	850	0.5~50m	MMF	YES	N/A	0℃~+70℃	PAM4

Note: 1 Case Temperature

Absolute Maximum Ratings

Table2- Absolute Maximum Ratings

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Storage Temperature	T_s	-10		+70	℃	
Supply Voltage	V_{CC}	-0.5		+3.6	V	
Operating Humidity	*RH*	+5		+85	%	1

Note: 1 No condensation

Recommended Operating Conditions

Table 3- Recommended operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Power Dissipation	P_d			10	W	1
Operating Case Temperature	T_c	0		+70	℃	
Bit Rate	*BR*		26.5625		GBd	2

Note:
1. Per terminal
2. Per channel, PAM4

Electrical Characteristics

Table 4- Electrical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Transmitter						
Signaling rate (each lane)	*SR*	26.5625 ± 100 ppm			GBd	
Differential data input voltage per lane	$V_{in,pp,diff}$	900			mV	
Differential termination mismatch	-			10	%	
Single-ended voltage tolerance range	-	-0.4		3.3	V	
DC common mode voltage	-	-350		2850	mV	
Receiver						

Signaling rate (each lane)	*SR*	26.5625 ± 100 ppm			GBd	
Differential output voltage	-			900	mV	
Near-end ESMW (Eye symmetry mask width)	-	0.265			UI	
Near-end Eye height, differential (min)	-	70			mV	
Far-end ESMW (Eye symmetry mask width)	-	0.2			UI	
Far-end Eye height, differential (min)	-	30			mV	
Differential termination mismatch	-			10	%	
Transition time (min, 20% to 80%)	-	9.5			ps	
DC common mode voltage	-	-350		2850	mV	
Bit Error Ratio	*BER*			2.4E-4		1

Note: 1 PRBS31Q@26.5625Gbd PAM4

Recommended Interface Circuit

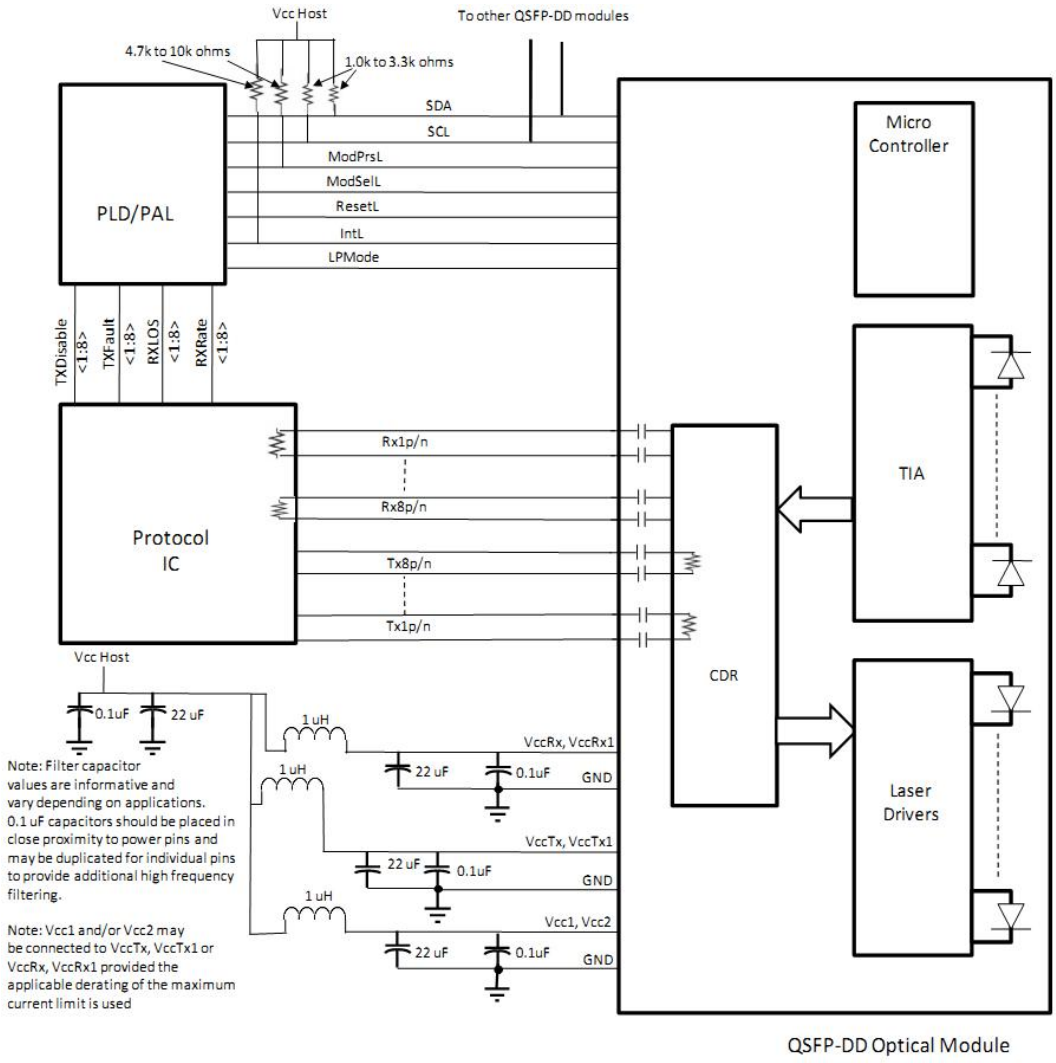
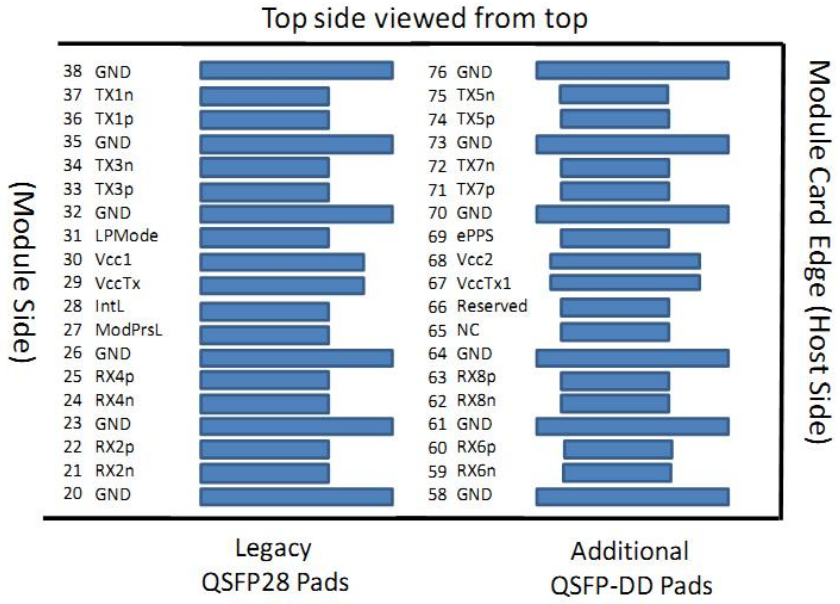


Figure 1, Recommended Interface Circuit

Pin arrangement



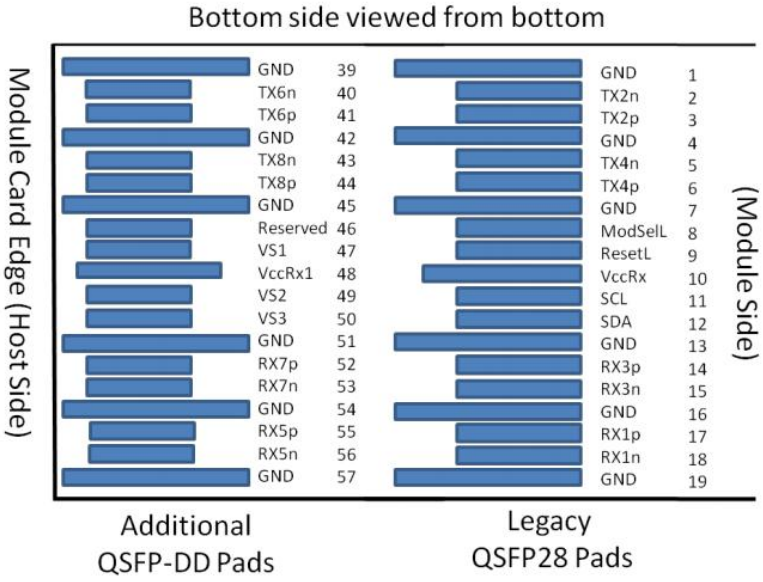


Figure 2, Pin View

Pin Function Definitions

Table 6-Pin Function Definitions

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1

8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		V_{CC} Rx	+3.3V Power Supply Receiver	2B	
11	LVCMOS-I/0	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/0	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-0	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-0	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-0	Rxlp	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rxln	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-0	Rx2n	Receiver Inverted Data Output	3B	
22	CML-0	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-0	Rx4n	Receiver Inverted Data Output	3B	
25	CML-0	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-0	ModPrsL	Module Present	3B	
28	LVTTL-0	IntL	Interrupt	3B	
29		V_{CC} Tx	+3.3V Power supply transmitter	2B	
30		V_{CC}l	+3.3V Power supply	2B	
31	LVTTL-I	LPMode	Low Power mode;	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Txlp	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Txln	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	
47		VS1	Module Vendor Specific 1	3A	
48		V_{CC} Rxl	3.3V Power Supply	2A	
49		VS2	Module Vendor Specific 2	3A	
50		VS3	Module Vendor Specific 3	3A	
51		GND	Ground	1A	1
52	CML-0	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-0	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-0	Rx5p	Receiver Non-Inverted Data Output	3A	

56	CML-0	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-0	Rx6n	Receiver Inverted Data Output	3A	
60	CML-0	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-0	Rx8n	Receiver Inverted Data Output	3A	
63	CML-0	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	
66		Reserved	For future use	3A	
67		V_{CC} Txl	3.3V Power Supply	2A	
68		$V_{CC}2$	3.3V Power Supply	2A	
69	LVTTL-I	ePPS	Precision Time Protocol (PTP) reference clock input	3A	
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Note: 1 Circuit ground is internally isolated from chassis ground.

Memory Map

Compatible with QSFP-DD CMIS rev 4.0.

Mechanical Outline Dimensions

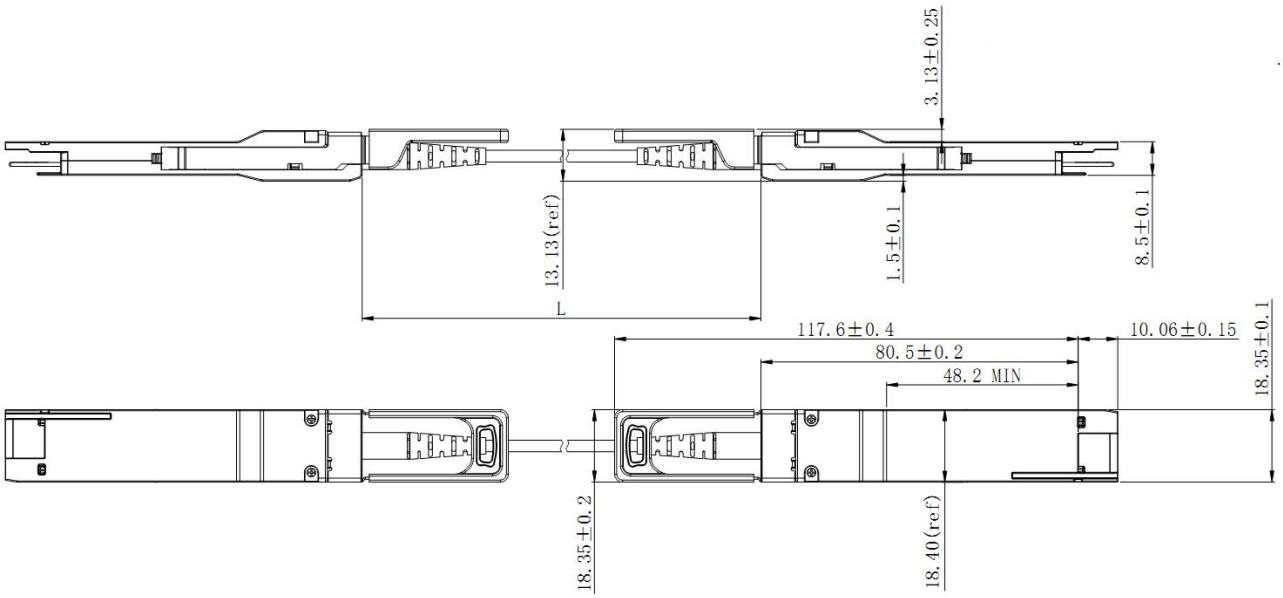


Figure3, Mechanical Diagram(Unit:mm)

Product list

Part Number	Product Name
1000XXXX	光模块_850nm_400G_QSFP-DD_AOC_Xm_MPO-16_1*8_J97