

200G QSFP56 SR4 CDR Optical Module

Product Specification Data

Product Name: QM_200G_QSFP56_SR4_CDR_Optical Module

Part Number: 10001704

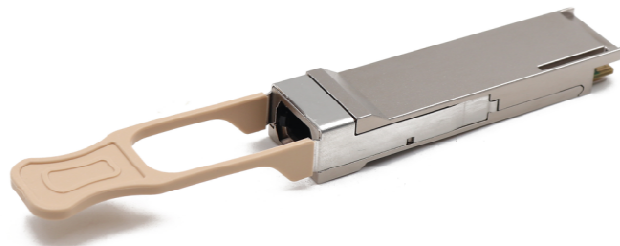
Record Number: TS09052

Version: A1

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Features

- Hot-pluggable QSFP form factor
- Case temperature range of 0°C to +70°C
- Maximum link length of 100m on OM4 fiber with KP4 FEC
- +3.3V single power supply
- Power dissipation < 4.5W with CDR
- Operating case temperature 0°C~70°C
- MPO-12 APC connector
- RoHS compliant



Applications

- 200GBASE-SR4 Ethernet

Standards

- Compliant to SFF-8636

ESD

- ESD compatible with MIL-STD-883 method 3015

Laser Safety

- Laser eye safety compatible with FDA 21CFR 1040.10 and 1040.11 EN60950, EN (IEC) 60825-1,2

Order Information

Table 1-Order Information

Part No.	Bit Rate (Gbps)	Laser (nm)	Distance ^{note1}	Fiber Type	DDMI	Connector	Temp ^{note2}
10001704	212.5	850	100m	MMF	YES	MPO 1x12 APC	0°C~+70°C

Note:

- OM4 fiber, 70m for OM3 fiber, with KP4 FEC
- Case Temperature

Absolute Maximum Ratings

Table2- Absolute Maximum Ratings

Parameters	Symbol	Min.	Typical	Max.	Unit	Notes
Storage Temperature	T_s	-40		+85	°C	
Supply Voltage	V_{CC}	-0.5		+3.6	V	
Operating Humidity	RH	+5		+85	%	1
Receiver Damage Threshold per Lane	P_{RDMG}	+5			dBm	

Note: 1 No condensation

Recommended Operating Condition

Table 3- Recommended operating Conditions

Parameters	Symbol	Min.	Typical	Max.	Unit	Notes
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Power Dissipation	P_d			4.5	W	
Operating Case Temperature	T_c	0		70	°C	

Electrical Characteristics

Table 4- Electrical Characteristics

Parameters	Symbol	Min.	Typical	Max.	Unit	Notes
Transmitter						
Signaling rate (each lane)	SR	26.5625 ± 100 ppm			GBd	
Differential data input voltage per lane	$V_{in,pp,diff}$			900	mV	
Differential termination mismatch	-			10	%	
Single-ended voltage tolerance range	-	-0.4		3.3	V	
DC common mode voltage	-	-350		2850	mV	
Receiver						
Signaling rate (each lane)	SR	26.5625 ± 100 ppm			GBd	
Differential output voltage	-			900	mV	

Near-end ESMW (Eye symmetry mask width)	-	0.265			UI	
Near-end Eye height, differential (min)	-	70			mV	
Far-end ESMW (Eye symmetry mask width)	-	0.2			UI	
Far-end Eye height, differential (min)	-	30			mV	
Differential termination mismatch	-			10	%	
Transition time (min, 20% to 80%)	-	9.5			ps	
DC common mode voltage	-	-350		2850	mV	

Optical Characteristics

Table 5-Optical Characteristics

Parameters	Symbol	Min.	Typical	Max.	Unit	Notes
Optical transmitter Characteristics						
Signaling rate (each lane)	SR	26.5625 ± 100 ppm			GBd	Per lane
Modulation format	-	PAM4			-	
Lane wavelength	λ	840	850	860	nm	
RMS spectral width	$\Delta\lambda$			0.6	nm	
Average launch power, each lane	-	-6.5		4	dBm	
Outer Optical Modulation Amplitude (OMA outer), each lane	-	-4.5		3	dBm	1
Launch power in OMA outer minus TDECQ, each lane	-	-5.9			dBm	
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane	-			4.5	dB	
Average launch power of OFF transmitter, each lane	-			-30	dBm	
Extinction ratio	-	3			dB	
Transmitter transition time, each lane	-			34	ps	
Optical return loss tolerance	-			12	dB	
Optical Receiver Characteristics						
Signaling rate (each lane)	SR	26.5625 ± 100 ppm			GBd	
Modulation format	-	PAM4			-	
Lane wavelength	λ	840	850	860	nm	
Damage threshold, each lane	P_{in}	5			dBm	
Average receive power, each lane	-	-8.4		4	dBm	
Receive power (OMA outer), each lane	-			3	dBm	
Receiver sensitivity (OMA outer), each lane	-			Max(6.5, SECQ-7.9)	dBm	2

LOS Assert	-	-30		-10	dBm	
LOS De-Assert	-			-9	dBm	
LOS Hysteresis	-	0.5			dB	

Note:

1. Even if the TDECQ < 1.4 dB, the OMA outer (min) must exceed this value.
2. Bit Error Ratio < 2.4×10^{-4} , Pattern PRBS31Q

Recommended Interface Circuit

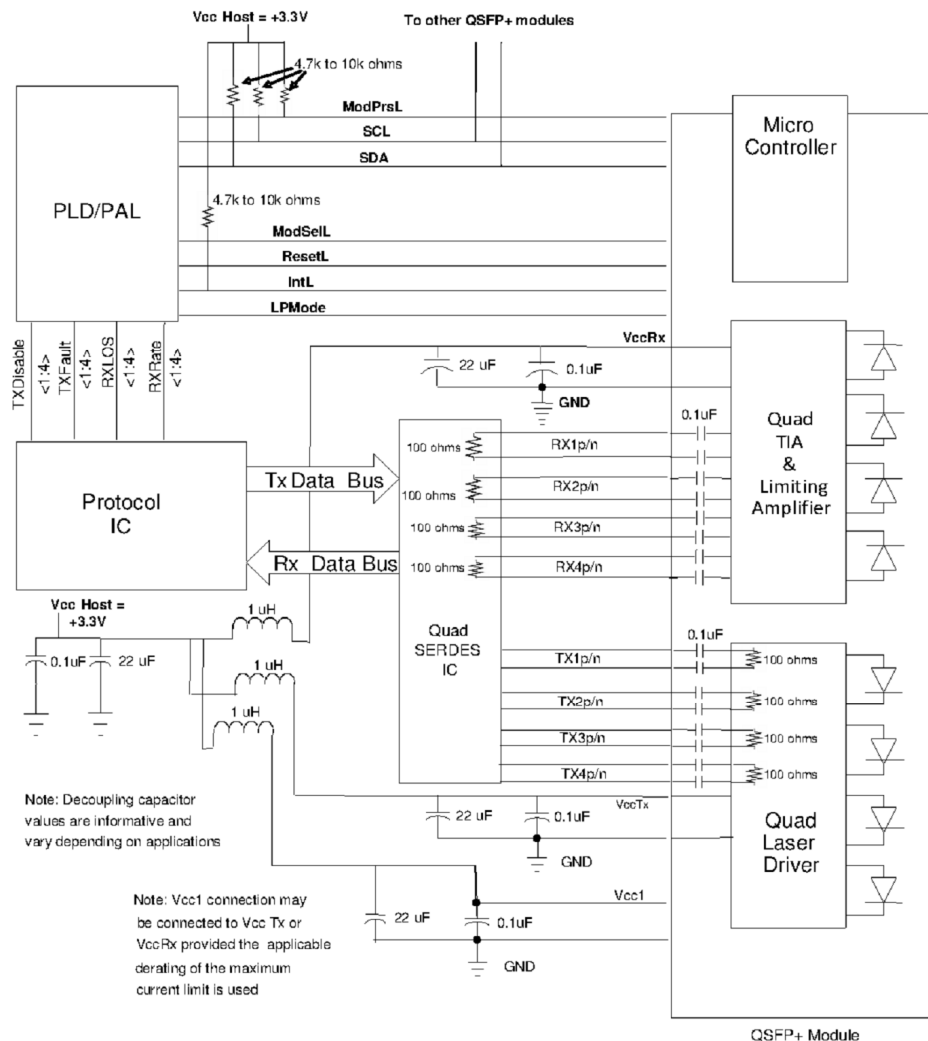


Figure 1, Recommended Interface Circuit

Pin arrangement

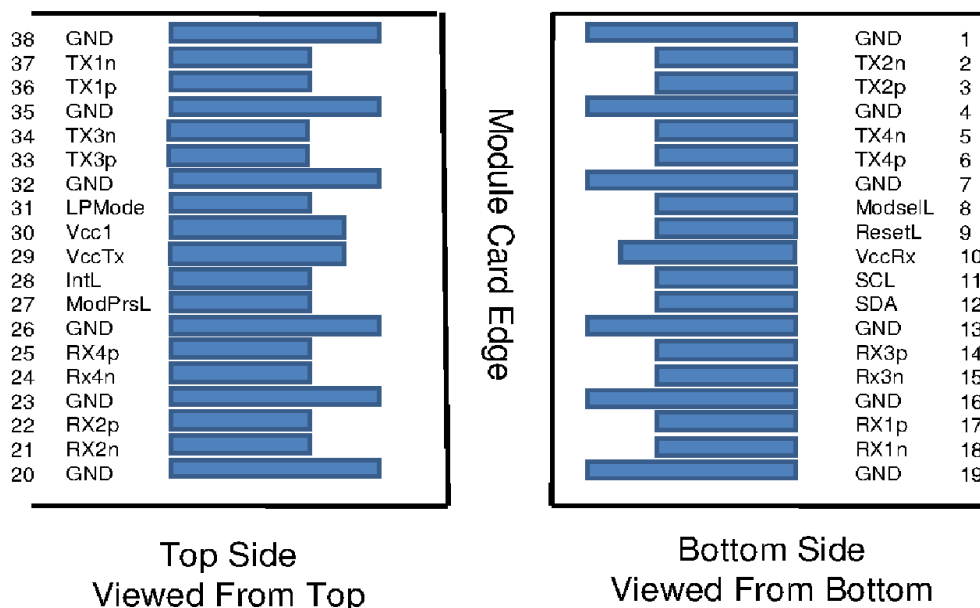


Figure 2, Pin View

Pin Function Definitions

Table 6-Pin Function Definitions

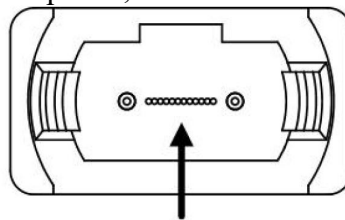
Pin	Logic	Symbol	Name/Description	Notes
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		V _{CC} Rx	+3.3V Power Supply Receiver	
11	LVC MOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVC MOS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Inverted Data Output	
15	CML-O	Rx3n	Receiver Non-Inverted Data Output	
16		GND	Ground	1

17	CML-O	Rx1p	Receiver Inverted Data Output	
18	CML-O	Rx1n	Receiver Non-Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		V _{CC} Tx	+3.3V Power Supply Transmitter	
30		V _{CC} 1	+3.3V Power Supply	
31	LVTTL-I	LPMODE	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Inverted Data Input	
34	CML-I	Tx3n	Transmitter Non-Inverted Data Input	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Inverted Data Input	
37	CML-I	Tx1n	Transmitter Non-Inverted Data Input	
38		GND	Ground	1

Note: 1 Circuit ground is internally isolated from chassis ground

Optical interface arrangement

The optical port is a male MPO connector receptacle, with fiber lane assignments as shown in Figure 3.



Fiber Number: 12 11 10 9 4 3 2 1

Transmit Channels: 1 2 3 4

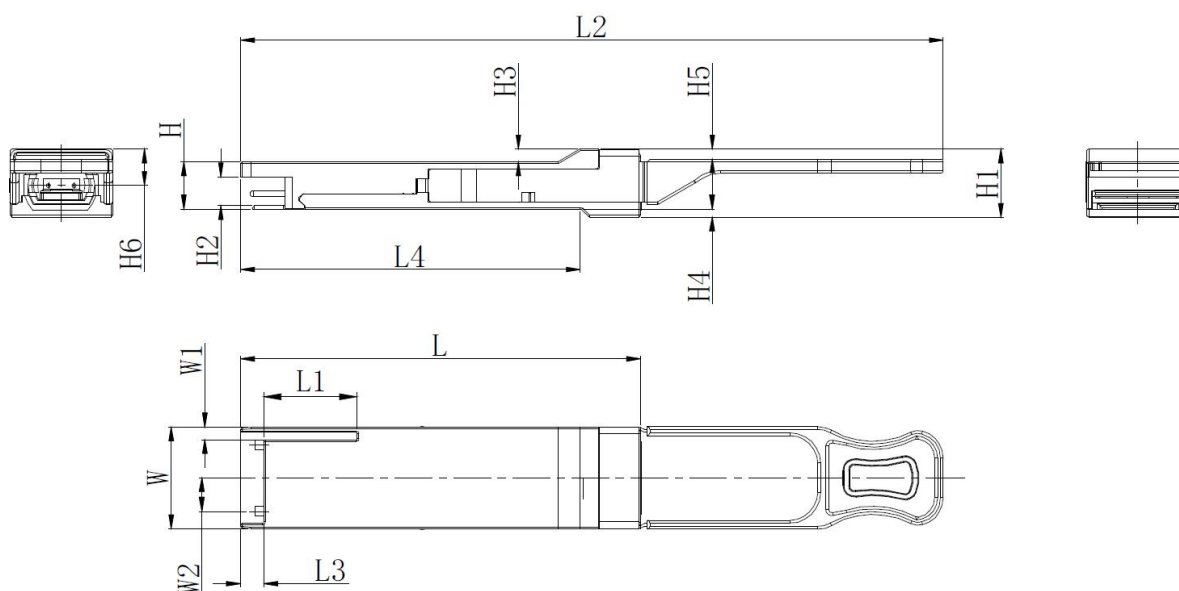
Receive Channels: 4 3 2 1

Figure 3, QSFP56 Optical Receptacle and Channel Orientation.

Monitoring Specification

Compatible with SFF-8636.

Mechanical Outline Dimensions



(Unit mm)

	L	L1	L2	L3	L4	W	W1	W2	H	H1	H2	H3	H4	H5	H6
Max	72.2	-	128	4.35	61.4	18.45	-	6.2	8.6	12.4	5.35	2.5	1.6	2.0	-
Type	72.0	-	-	4.20	61.2	18.35	-	-	8.5	12.2	5.2	2.3	1.5	1.8	6.55
Min	68.8	16.5	124	4.05	61.0	18.25	2.2	5.8	8.4	12.0	5.05	2.1	1.3	1.6	-

Figure 4, Mechanical Diagram

Product list

Part Number	Product Name
10001704	光模块_850nm_200G_QSFP56_SR4_100m_MPO-12_1*4_J97